

5  
4  
3  
2  
1

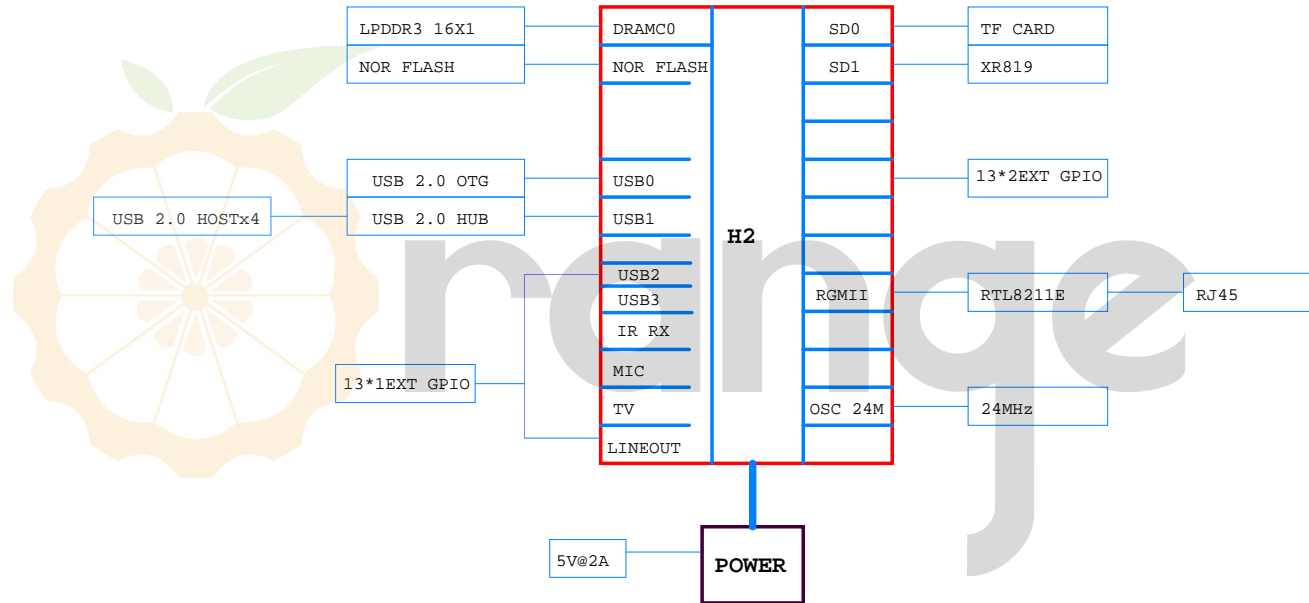
# REVISION HISTORY

Schematics Index:

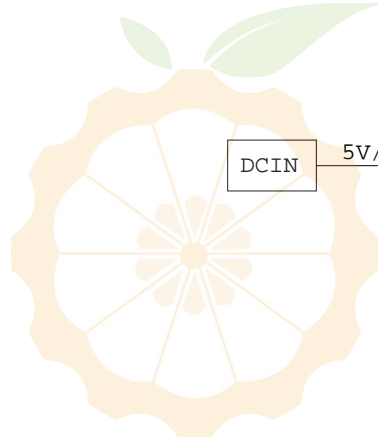
Revision	Description	Date	Drawn	Checked
Ver 1.0	Initial	2016-09-05		
1、主控晶振和匹配电容（WIFI）？ 2、POE供电				
Ver 1.1				
1、去掉WIFI部分π型滤波 2、串口调试更改为3pin 3、bom默认无POE供电（需要选焊）				
Ver 1.2				
1、简化WIFI部分的电路，WC11容值更改为0.22uF				
Ver 1.3				
Ver 1.4				
Ver 1.5				
1、更改供电逻辑，减弱对WIFI的干扰				



range pi



POWER TREE



DCIN

5V/2A

SY8008B

3.3V/300mA

AVCC/RTC

SY8008B

1.5V/1A

DRAM

SY8089A

1.2V/2A

SYSTEM

SY8113B

1.3V/3A

VCC-CPUX

SY8008B

3.3V/0.8A

VCC-IO

PST73133BETV

3.3V/0.8A

VCC-WIFI



Xunlong Software Co., Limited

Design Name ORANGE\_PI-Zero

Size A3 Page Name POWER TREE Rev 1.5

Date: Tuesday, February 18, 2019 Sheet 3 of 12

# GPIO ASSIGNMENT

PIN	Define	CFG	Function
PA0	I2S/DRVVBUS0	3/1	JTAG /USB
PA1	ICK/DRVVBUS1	3/1	
PA2	TDO/WPS	3/1	
PA3	TDI	3	UART
PA4	JART-TX	3	
PA5	JART-RX	3	
PA6	NC	7	
PA7	NC	7	
PA8	NC	7	
PA9	NC	7	
PA10	NC	7	
PA11	NC	7	
PA12	NC	7	
PA13	NC	7	
PA14	NC	7	
PA15	STATUS-LED	1	LED
PA16	MUTE	1	AV
PA17	SPDIF-OUT	2	SPDIF
PA18	NC	7	
PA19	NC	7	
PA20	NC	7	
PA21	NC	7	

PIN	Define	CFG	Function
PC0	NWE	2/3	NAND /eMMC /NOR
PC1	NALE	2/3	
PC2	NCLE	2/3	
PC3	NCE1	2/3	
PC4	NCE0	2	
PC5	NRE	2/3	
PC6	NRB0	2/3	
PC7	NRB1	2	
PC8	NDQ0	2/3	
PC9	NDQ1	2/3	
PC10	NDQ2	2/3	
PC11	NDQ3	2/3	
PC12	NDQ4	2/3	
PC13	NDQ5	2/3	
PC14	NDQ6	2/3	
PC15	NDQ7	2/3	
PC16	NDQS	2/3	

PIN	Define	CFG	Function
PD0	NC	7	
PD1	NC	7	
PD2	NC	7	
PD3	NC	7	
PD4	NC	7	
PD5	NC	7	
PD6	NC	7	
PD7	NC	7	
PD8	NC	7	
PD9	NC	7	
PD10	NC	7	
PD11	NC	7	
PD12	NC	7	
PD13	NC	7	
PD14	NC	7	
PD15	NC	7	
PD16	NC	7	
PD17	NC	7	

PIN	Define	CFG	Function
PE0	NC	7	
PE1	NC	7	
PE2	NC	7	
PE3	NC	7	
PE4	NC	7	
PE5	NC	7	
PE6	NC	7	
PE7	NC	7	
PE8	NC	7	
PE9	NC	7	
PE10	NC	7	
PE11	NC	7	
PE12	NC	7	
PE13	NC	7	
PE14	NC	7	
PE15	NC	7	

PIN	Define	CFG	Function
PF0	D1	2	CARD0
PF1	D0	2	
PF2	CLK	2	
PF3	CMD	2	
PF4	D3	2	
PF5	D2	2	
PF6	DET	0	

PIN	Define	CFG	Function
PG0	NC	7	
PG1	NC	7	
PG2	NC	7	
PG3	NC	7	
PG4	NC	7	
PG5	NC	7	
PG6	NC	7	
PG7	NC	7	
PG8	NC	7	
PG9	NC	7	
PG10	NC	7	
PG11	NC	7	
PG12	NC	7	
PG13	NC	7	

PIN	Define	CFG	Function
PL0	TWI	2	TWI
PL1	TWI	2	
PL2	USB0-DRVVBUS	1	USB
PL3	USB1-DRVVBUS	1	
PL4	RECOVERY	0	KEY
PL5	VCC-IO-EN	1	IO-EN
PL6	NC	7	WIFI-EN
PL7	WIFI-EN	7	
PL8	PWR-STB	1	
PL9	PWR-DRAM	1	
PL10	PWR-LED	1	
PL11	IR-RX	2	

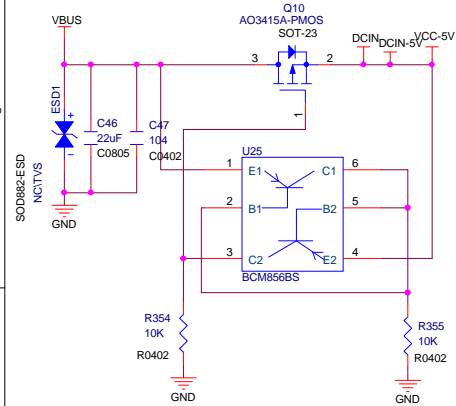
## 4



## 1



## DCIN

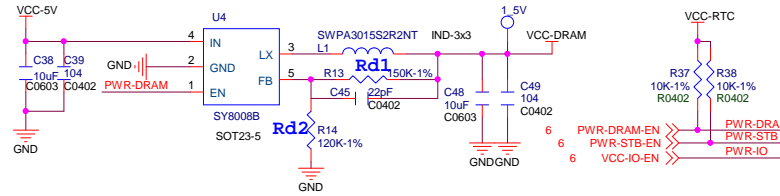


## POWER

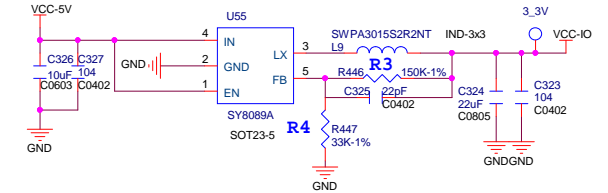
$$V_{out} = 0.6 * (1 + R_{d1} / R_{d2})$$

$$V_{DRAM} = 1.5V / 1A, R_2 = 100K - 1\%$$

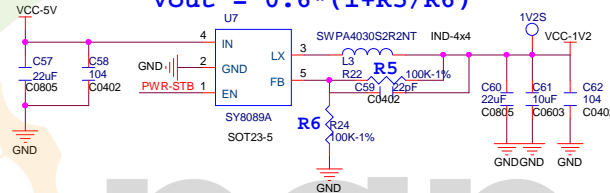
$$V_{DRAM} = 1.35V / 1A, R_2 = 120K - 1\%$$



## VCCIO 3.3V/2A



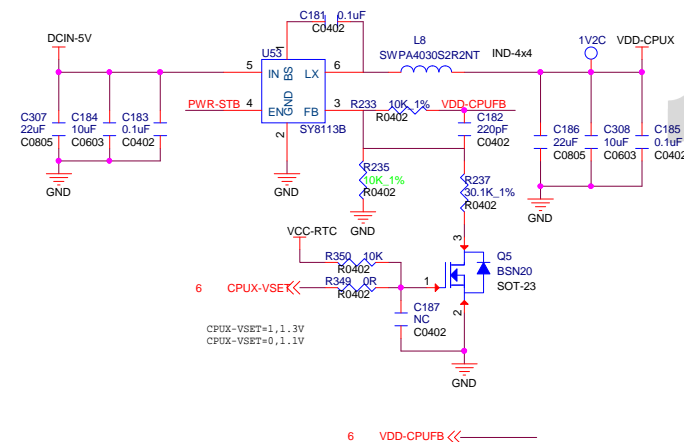
## SYSTEM 1.2V/2A

$$V_{out} = 0.6 * (1 + R_5 / R_6)$$


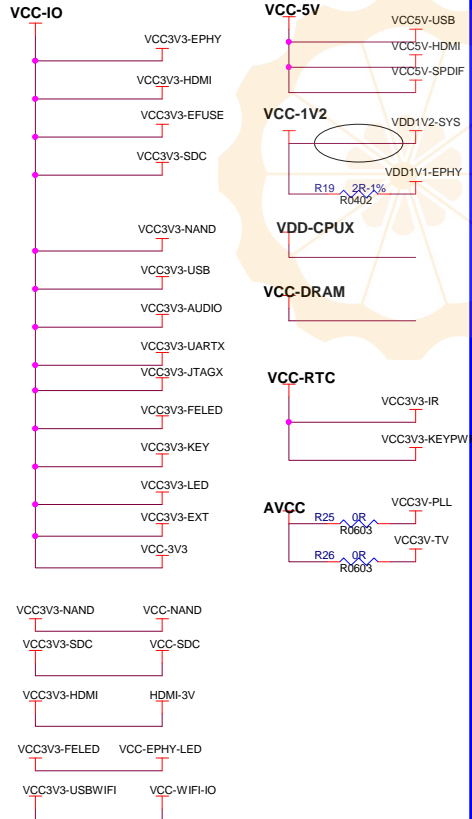
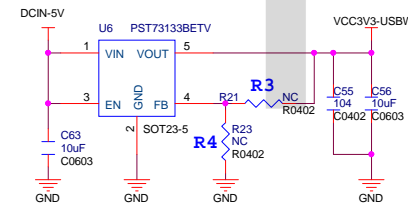
## AVCC 3.3V/1A



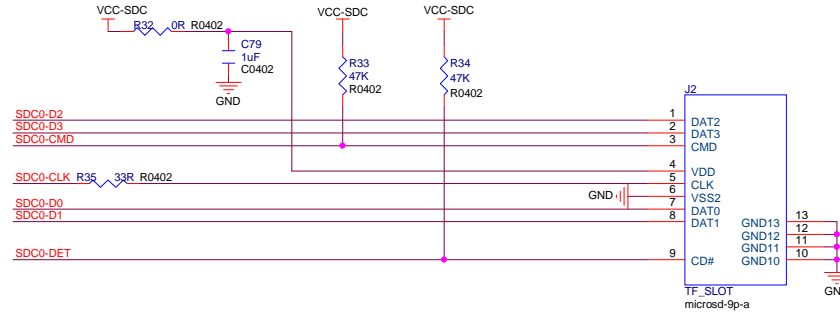
## CPUX 1.1V/1.3V/3A

$$V_{out} = 0.6 * (1 + R_1 / R_2)$$


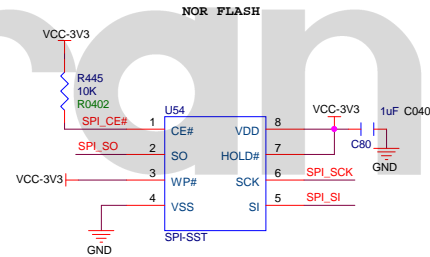
## WIFI Power 3.3V/300mA



## eMMC



## NOR FLASH





# USB

5

4

3

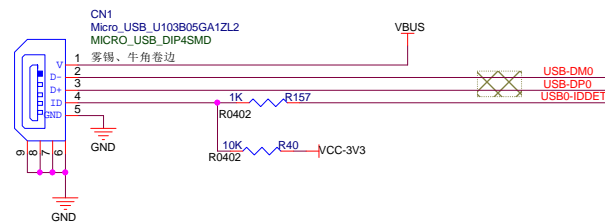
2

1

D

D

6 USB-DM0  
6 USB-DP0  
6 USB0-IDDET  
6 USB0-DRVVBUS

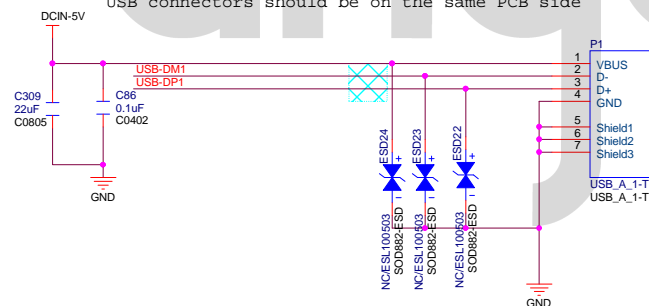


C

C

6 USB-DM1  
6 USB-DP1

note: Make sure the routing between the ESD and the USB connectors should be on the same PCB side



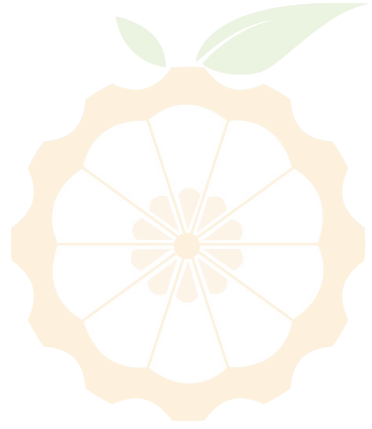
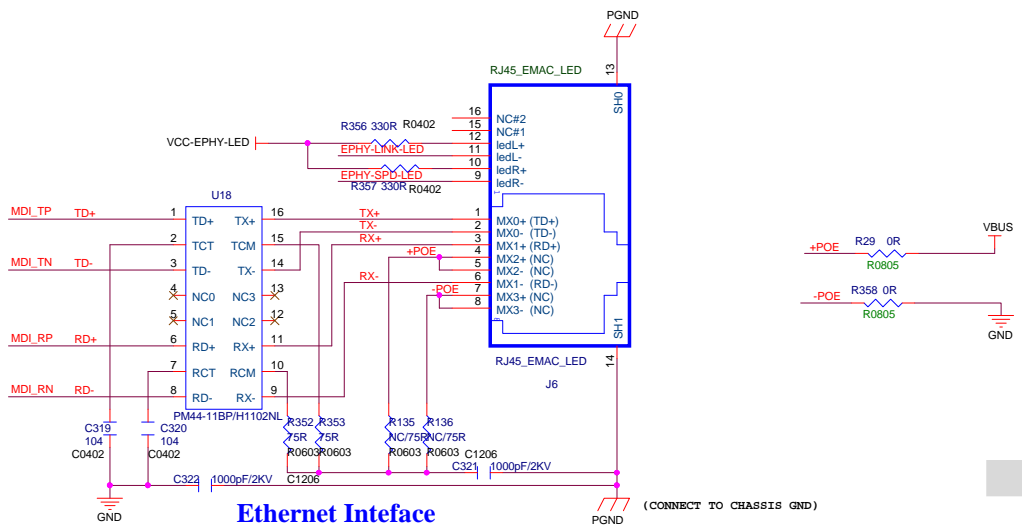
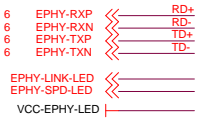
B

B

A

A

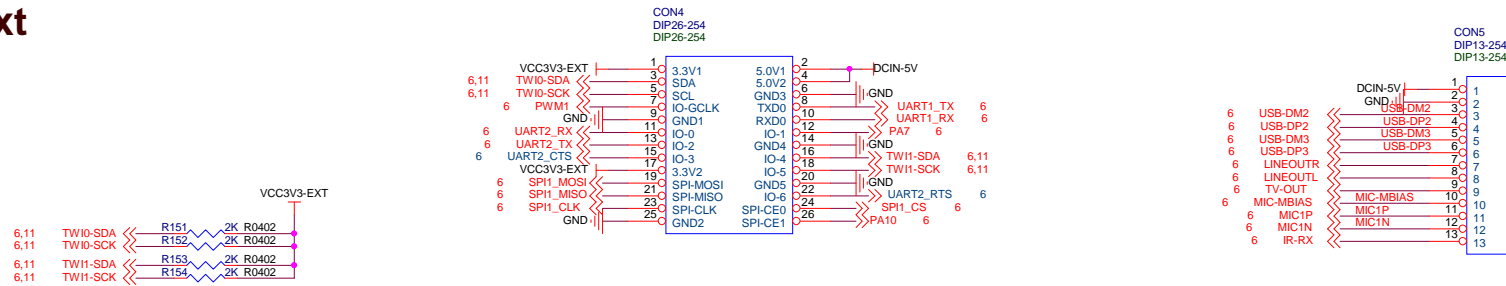
# EMAC



range pi

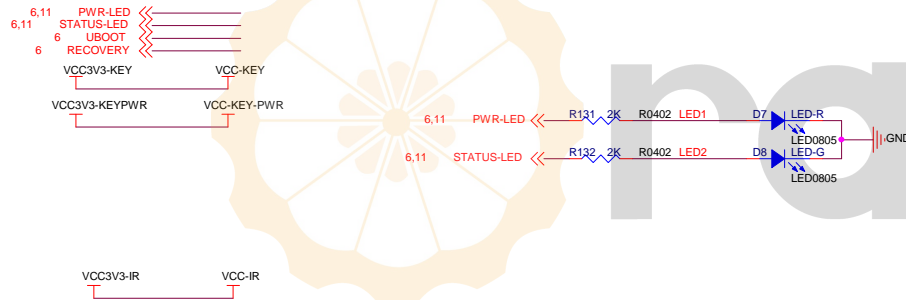
## Ext Port

### Ext

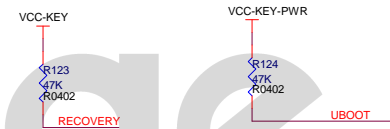


USB\*2 @ AUDIO @ IR

### LED



### KEY

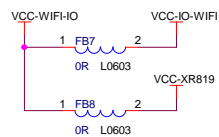


### DEBUG

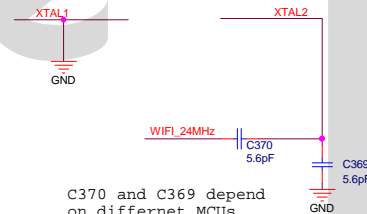
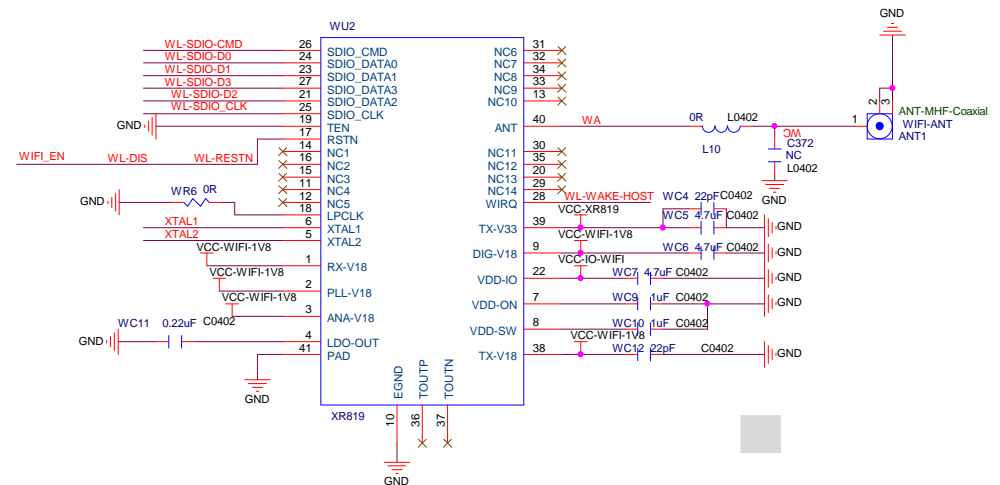


Xunlong Software Co., Limited			
Design Name			
ORANGE_PI-Zero			
Size	Page Name	Rev	
A3	EXT	1.5	
Date:	Tuesday, February 19, 2019	Sheet	11 of 12

## 1



# XR819 ON BOARD



C370 and C369 depend  
on different MCHs

注：  
WC13焊接0R电阻，C370焊接5.6pF，  
C369焊接5.6pF

注：主控晶振和匹配电容需要适配；  
参考：  
主控晶振选用型号：JWT24.000  
主控晶振匹配电容改为：  
XC31焊接27pF，  
XC41焊接12pF

